**REMARKS**

Claims 1-4, 6-9, 11-13, 16-17, 19-22, 32, 34-35, 38, 40-41, 44, 46-47, 50, 52-53, 56, and 59-64 remain pending in the application. Claims 23-31 and 58 have been canceled without prejudice or disclaimer. Favorable reconsideration is respectfully requested in view of the above amendments and the following remarks.

Claims 1-4, 6-9, 11-13, 16-17, 19-22, 32, 34-35, 38, 40-41, 44, 46-47, 50, 52-53, 56, and 59-64 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Taylor et al. (US 5,463,732) in view of Campbell et al (US 5,021,947). This rejection is respectfully traversed.

Taylor describes prior art attempts at processing lines of video data. In essence, a prior art parallel processor comprises a plurality of processor units, each associated with its own local memory. A line of input video data is temporarily buffered in a distributed buffer consisting of the memories of the individual processors. Each pixel forming such a line is passed to a respective processor unit. On the occurrence of a horizontal sync signal being detected, all of the processors are reset to zero and a main processing function is performed. Typical examples include filtering, image rotation, image scaling etc. as per Col 2, lines 2-8 of Taylor. The memories also act as a distributed output buffer, enabling a processed video line to be held temporarily until a whole video frame has been processed, at which time the frame is output to a display device. The ratio of processor clock speed to line display rate sets what is called an "instruction budget", which dictates the ability (or otherwise) of the parallel processor to process the video data in real time. In the case of a processor that is unable to process a frame within the budget, a processed frame may be displayed repetitively (refreshed) until such time as the processor has managed to process a new complete frame. This requires a frame monitor to indicate when such a new frame is ready for output to the display device.

The prior art system described in Taylor is unsatisfactory in that access to the frame data in the distributed memory/buffer of the parallel processor must either (a) be accomplished within the instruction budget or (b) there must be a frame monitor. The problem to be solved by Taylor is acknowledged in Col 3, lines 46-50 as being the provision of a method and apparatus for accessing a distributed data buffer in a parallel processing computer that does not impact the nature and function of a MAIN routine that accomplishes data processing.

The processor forming the subject of the invention described by Taylor aims to solve those problems by temporarily interrupting the MAIN processing routine so as to enable the data stored in the distributed buffer to be output. The inventive concept in Taylor appears to be that the status of the processor is also stored so that, when the interrupt ceases, the MAIN routine can continue from the point it had reached when the interrupt occurred.

Taylor describes in Col 5, lines 25 onwards, a processor subsystem or unit depicted in Figure 2. The unit receives a digital video signal (a serial data stream) which is distributed amongst the processor subsystems by means of a cascade of shift registers, each of which is capable of storing a single pixel value. The input buffer depth is stated in Col 5, lines 48-49 to be "application specific". As with the prior art system described by Taylor, an entire frame is buffered. This too is said to be application specific (Col 5, lines 57-58). One line of processed data at a time is output to an output register from local memory until a whole frame has been transferred. The frame is then output as a serial stream (Col 6, lines1-15).

Interruption of the MAIN routine occurs for a variety of reasons, such as output buffer swapping (Col 6, lines 50-66). During this time, the MAIN routine is in "hold" until the interrupt is completed and the MAIN routine restarted from where it was interrupted. The actual details of the interrupt operation are not relevant to the present invention and to the Office's objection on the grounds of alleged obviousness.

It is therefore clear that each processing unit of the Taylor processor handles only a single pixel at any given time. Moreover, those pixels are of known, predetermined, invariable size. Even further, there is absolutely no concept disclosed, suggested or even vaguely hinted at in Taylor that the pixels constitute part of a packet. On the contrary, the pixels form part of a serial data stream, each data item representing a pixel value. In the absence of such a suggestion, there is no motivation for the skilled person to contemplate that the pixel values were or might be values of a packet consisting of a plurality of pixel values or that each video line constituted a packet. If pixels are equated with packets (i.e., one pixel per packet), there will be one or possibly a fixed number of pixels per processor and possibly another set waiting in an input or output buffer, On the other hand, if a line of pixels is regarded as equivalent to a packet, the same argument applies in that there are a fixed number of pixels allocated to a fixed number of processors. The number of processors in the hardware is defined by the size of the line. There is therefore no dynamic (run time) allocation of the number of processors actually used.

Yet further, Taylor's processing system is acknowledged to be application specific, so it will be designed for a given, fixed, predetermined, invariable size of data item (pixel) so there is no invitation to the skilled person to consider any other data options, and certainly not "data packets of unpredictable size", as recited in Applicants' independent claim 1. Even yet further, there is absolutely no necessity for any thought to be given to dynamic distribution of the data stream based, at least in part, on the size of the data, as would further be required to satisfy the terms of Applicants' independent claim 1. Finally, the problems that Taylor attempts to solve are completely unrelated to those addressed in the present invention. Taylor wants to provide a processor system that overcomes the problems of the prior art where access to frame data in the distributed memory/buffer of the parallel processor must either be accomplished within the instruction budget or alternatively there must be a frame monitor.

Despite this being the position as regards the teaching of Taylor, the Office suggests that the skilled person would be drawn to Campbell to fill the gaps not met by Taylor. In this regard, the Office suggests that Campbell discloses a variable packet size and a dynamic determination of PE number according to packet length. The various reasons stated in the Office Action for the skilled person being so motivated are not relevant to the present invention and to its objectives. First, the suggestion that Campbell could provide Taylor with the control capability to distribute the data depending on the number of processing elements is beside the point because it is only with an improper hindsight analysis that the skilled person would even contemplate distributing data depending on the number of processing elements. Likewise, minimizing the conflict among the processing elements is not an issue with the prior art, either with Taylor or with Campbell. Obtaining the necessary control capability is a consideration **after** the concept of dynamic determination of distribution of packets of unpredictable size has arisen. Second, the fact that Taylor taught n pixel values with two swapped buffers (not packet buffers, contrary to the Office's suggestion) cannot be seen as a suggestion as to the need for determining the number of PEs based on a predictable size. The swapped buffer arrangement in Taylor is simply a means for handling one group of data (output frame data) while a fresh frame of data is being processed from new input data, ready to be placed in one of the two output buffers when the current contents have been output to the display device.

Looking at the position from the reverse perspective, Campbell is not a valid starting point for an obviousness objection. The person of ordinary skill in the art would not have been motivated to combine Campbell with Taylor for a number of reasons. Firstly, Campbell

teaches a technique for allocating program code, not data, to processors. This is quite a distinct difference and is one that is recognized in the art as being an extremely difficult problem to solve. There are multiple constraints to be resolved, each of which requires a complex analysis of the program execution and the data dependencies within it. Finally, this allocation is done once, at compile time, not dynamically at run time as in Applicants' invention. If the person of ordinary skill in the art were looking for a simple method to dynamically partition data across a set of processors, Campbell would be dismissed instantly as being too complex and irrelevant. If that were not enough to deter the person of ordinary skill, Campbell explicitly states that each packet has the PE address and that the packet is sent to that PE. The "actor" (piece of program code) on that PE will need the entire packet on that PE in order to process it. Campbell is therefore yet further distanced from Applicants' invention.

With respect to the Office's arguments for "motivation", we cannot see that any of those arguments are relevant to the inventive contribution of the present application, namely the dynamic distribution of incoming data packets of unpredictable size to a number of non-predicated processing elements on the basis, at least in part, of packet size. As mentioned in our previous response, the number of processing elements may vary according to the data and it may be the case that not all of the processing elements are used at any one time. The present invention does not need any authority or prior knowledge of the incoming data packet stream. Packet distribution is "on the fly", contrary to any suggestion, implicit or otherwise, in Taylor or in Campbell. With respect, we believe the Office's arguments are purely *de post facto* and cannot reasonably be said to have any origin in the teaching of Taylor or Campbell, alone or together. The passage referred to by the Office in Column 8 of Campbell undoubtedly mentions packets having two different sizes or even variable-length packets but that is not the end of the story since there is no subsequent disclosure or suggestion that such packets are distributed, according to their size, over any number of PEs necessary to store them, as is required of Applicants' claims.

It is respectfully contended that Taylor does not constitute a valid starting point for the obviousness objection and Campbell does not provide the missing links to arrive at Applicants' claimed invention without the benefit of a considerable amount of hindsight. Equally, as explored above, Campbell does not provide a valid starting point either.

It is therefore respectfully contended that independent claim 1, as currently drawn, is not in fact rendered obvious by the combination of Campbell with Taylor, whichever of these

is treated as a starting point. The dependent claims 2-4, 6-9, 11-13, 16-17, 19-22, 32, 34-35, 38, 40-41, 44, 46-47, 50, 52-53, 56, and 59-64 inherit the features of independent claim 1, and are therefore patentably distinguishable over any combination of Taylor with Campbell for at least the same reasons as set forth above. It is therefore respectfully requested that the rejection of claims 1-4, 6-9, 11-13, 16-17, 19-22, 32, 34-35, 38, 40-41, 44, 46-47, 50, 52-53, 56, and 59-64 under 35 U.S.C. §103(a) be withdrawn.

The application is believed to be in condition for allowance. Prompt notice of same is respectfully requested.

Respectfully submitted,

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